

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first conductive type of first MOS transistor  
which is formed in a first active area and in which  
5 a gate is configured from a first gate electrode, the  
first gate electrode having an end portion projecting  
from the first active area;

a second active area arranged adjacent to the  
first active area;

10 a second conductive type of second MOS transistor  
which is formed in the second active area and in which  
a gate is configured from the first gate electrode;

a second conductive type of third MOS transistor  
which is formed in the second active area and in which  
15 a gate is configured from a second gate electrode;

a third active area formed apart from the first  
active area;

a first conductive type of fourth MOS transistor  
which is formed in the third active area and in which  
20 a gate is configured from a third gate electrode, the  
third gate electrode having an end portion projecting  
from the third active area;

a fourth active area arranged adjacent to the  
third active area;

25 a second conductive type of fifth MOS transistor  
which is formed in the fourth active area and in which  
a gate is configured from the third gate electrode; and

a second conductive type of sixth MOS transistor which is formed in the fourth active area and in which a gate is configured from a fourth gate electrode,

wherein the end portion of the first gate  
5 electrode projecting from the first active area is obliquely arranged relative to a gate width direction of the first MOS transistor, and the end portion of the third gate electrode projecting from the third active area is obliquely arranged relative to a gate width  
10 direction of the fourth MOS transistor.

2. A semiconductor device according to claim 1, wherein the first gate electrode has an end portion projecting from the second active area, the third gate electrode has an end portion projecting from the fourth  
15 active area, the end portion of the first gate electrode projecting from the second active area is obliquely arranged relative to a gate width direction of the second MOS transistor, and the end portion of the third gate electrode projecting from the fourth  
20 active area is obliquely arranged relative to a gate width direction of the fifth MOS transistor.

3. A semiconductor device according to claim 2, wherein the second gate electrode has an end portion projecting from the second active area, the fourth gate  
25 electrode has an end portion projecting from the fourth active area, the end portion of the second gate electrode projecting from the second active area is

obliquely arranged relative to a gate width direction  
of the third MOS transistor, and the end portion of the  
fourth gate electrode projecting from the fourth active  
area is obliquely arranged relative to a gate width  
5 direction of the sixth MOS transistor.

4. A semiconductor device according to claim 1,  
wherein the first, second, and third MOS transistors  
are arranged in point symmetry on the basis of  
a central point between the first MOS transistor and  
10 the fourth MOS transistor relative to the fourth,  
fifth, and sixth MOS transistors.

5. A semiconductor device according to claim 4,  
wherein the first to sixth transistors configure  
a rectangular unit cell and other unit cells are  
15 arranged in line symmetry on the basis of each side of  
the unit cell outside the unit cell.

6. A semiconductor device according to claim 5,  
wherein the end portion of the first gate electrode  
projecting from the first active area and the end  
20 portion of the third gate electrode projecting from  
the third active area are obliquely arranged relative  
to a long side direction of the unit cell.

7. A semiconductor device according to claim 1,  
further comprising;  
25 a first shared contact which is commonly connected  
to the end portion of the first gate electrode  
projecting from the first active area and the third

active area, and

a second shared contact which is commonly  
connected to the end portion of the third gate  
electrode projecting from the third active area and the  
first active area.

8. A semiconductor device according to claim 7,  
wherein a major axis of the first shared contact and  
the end portion of the first gate electrode projecting  
from the first active area are arranged in the same  
direction, and

a major axis of the second shared contact and the  
end portion of the third gate electrode projecting from  
the third active area are arranged in the same  
direction.

9. A semiconductor device according to claim 1,  
wherein the first to fourth active areas are formed on  
an insulating film.

10. A semiconductor device comprising:

a first active area formed in an isolation area;

a first conductive type of first MOS transistor  
which is formed in the first active area and in which  
a gate is configured from a first gate electrode, the  
first gate electrode having an end portion which  
projects from the first active area and resides in the  
isolation area;

a second active area arranged adjacent to the  
first active area in the isolation area;

a second conductive type of second MOS transistor which is formed in the second active area and in which a gate is configured from the first gate electrode;

5 a second conductive type of third MOS transistor which is formed in the second active area and in which a gate is configured from a second gate electrode;

a third active area formed apart from the first active area in the isolation area;

10 a first conductive type of fourth MOS transistor which is formed in the third active area and in which a gate is configured from a third gate electrode, the third gate electrode having an end portion which projects from the third active area and resides in the isolation area;

15 a fourth active area which is arranged adjacent to the third active area in the isolation area;

a second conductive type of fifth MOS transistor which is formed in the fourth active area and in which a gate is configured from the third gate electrode; and

20 a second conductive type of sixth MOS transistor which is formed in the fourth active area and in which a gate is configured from a fourth gate electrode,

wherein the end portion of the first gate electrode present in the isolation area is obliquely  
25 arranged relative to an extended direction of the first gate electrode arranged on the first active area, and the end portion of the third gate electrode present in

the isolation area is obliquely arranged relative to an extended direction of the third gate electrode arranged on the third active area.

11. A semiconductor device according to claim 10,  
5 wherein the first gate electrode has an end portion which projects from the second active area and resides in the isolation area, the third gate electrode has an end portion which projects from the fourth active area and resides in the isolation area, the end portion  
10 of the first gate electrode projecting from the second active area is obliquely arranged relative to a gate width direction of the second MOS transistor, and the end portion of the third gate electrode projecting from the fourth active area is obliquely arranged relative  
15 to a gate width direction of the fifth MOS transistor.

12. A semiconductor device according to claim 11,  
wherein the second gate electrode has an end portion which projects from the second active area and resides in the isolation area, the fourth gate electrode has  
20 an end portion which projects from the fourth active area and resides in the isolation area, the end portion of the second gate electrode projecting from the second active area is obliquely arranged relative to a gate width direction of the third MOS transistor, and the  
25 end portion of the fourth gate electrode projecting from the fourth active area is obliquely arranged relative to a gate width direction of the sixth MOS

transistor.

13. A semiconductor device according to claim 10,  
wherein the first, second, and third MOS transistors  
are arranged in point symmetry on the basis of  
5 a central point between the first MOS transistor and  
the fourth MOS transistor relative to the fourth,  
fifth, and sixth MOS transistors.

14. A semiconductor device according to claim 13,  
wherein the first to sixth MOS transistors configure  
10 a rectangular unit cell and other unit cells are  
arranged in line symmetry on the basis of each side of  
the unit cell outside the unit cell.

15. A semiconductor device according to claim 14,  
wherein the end portion of the first gate electrode  
15 projecting from the first active area and the end  
portion of the third gate electrode projecting from  
the third active area are obliquely arranged relative  
to a long side direction of the unit cell.

16. A semiconductor device according to claim 10,  
20 further comprising;

a first shared contact which is commonly connected  
to the end portion of the first gate electrode  
projecting from the first active area and the third  
active area, and

25 a second shared contact which is commonly  
connected to the end portion of the third gate  
electrode projecting from the third active area and

the first active area.

17. A semiconductor device according to claim 16,  
wherein a major axis of the first shared contact and  
the end portion of the first gate electrode projecting  
5 from the first active area are arranged in the same  
direction, and

a major axis of the second shared contact and the  
end portion of the third gate electrode projecting from  
the third active area are arranged in the same  
10 direction.

18. A semiconductor device according to claim 10,  
wherein the first to fourth active areas are formed on  
an insulating film.

19. A semiconductor device comprising:  
15 a first conductive type of first MOS transistor  
which is formed in a first active area and in which  
a gate is configured from a first gate electrode, the  
first active area including a diffusion layer which is  
connected to a contact supplied with power supply  
20 voltage and a diffusion layer on a node side of the  
first MOS transistor, which is arranged on an opposite  
side of the diffusion layer;

a second active area arranged adjacent to the  
first active area;

25 a second conductive type of second MOS transistor  
which is formed in the second active area and in which  
a gate is configured from the first gate electrode;



a second conductive type of third MOS transistor which is formed in the second active area and in which a gate is configured from a second gate electrode;

5 a third active area formed apart from the first active area;

a first conductive type of fourth MOS transistor which is formed in the third active area and in which a gate is configured from a third gate electrode, the third active area including a diffusion layer which is  
10 connected to a contact supplied with power supply voltage and a diffusion layer on a node side of the first MOS transistor, which is arranged on an opposite side of the diffusion layer;

15 a fourth active area arranged adjacent to the third active area;

a second conductive type of fifth MOS transistor which is formed in the fourth active area and in which a gate is configured from the third gate electrode; and

20 a second conductive type of sixth MOS transistor which is formed in the fourth active area and in which a gate is configured from a fourth gate electrode,

wherein the first to sixth MOS transistors configure a rectangular unit cell, a longitudinal direction of the diffusion layer on the node side of  
25 the first MOS transistor and a long side direction of the unit cell are arranged at an angle of 20 to 30 degrees from each other, and

a longitudinal direction of the diffusion layer on the node side of the fourth MOS transistor and the long side direction of the unit cell are arranged at an angle of 20 to 30 degrees from each other.

5           20. A semiconductor device according to claim 19, wherein the first, second, and third MOS transistors are arranged in point symmetry on the basis of a central point between the first MOS transistor and the fourth MOS transistor relative to the fourth, fifth,  
10           and sixth MOS transistors.

          21. A semiconductor device according to claim 20, wherein other unit cells are arranged in line symmetry on the basis of each side of the unit cell outside the unit cell which consists of the first to sixth MOS  
15           transistor.

          22. A semiconductor device according to claim 19, wherein the first gate electrode has an end portion projecting from the first active area, the third gate electrode has an end portion projecting from the third  
20           active, the end portion of the first gate electrode projecting from the first active area and the end portion of the third gate electrode projecting from the third active area are obliquely arranged relative to a long side direction of the unit cell.

25           23. A semiconductor device according to claim 19, wherein the first gate electrode has an end portion projecting from the first active area, and the third

gate electrode has an end portion projecting from the third active, the semiconductor device further comprising:

5 a first shared contact which is commonly connected to the end portion of the first gate electrode projecting from the first active area and the third active area; and

10 a second shared contact which is commonly connected to the end portion of the third gate electrode projecting from the third active area and the first active area.

15 24. A semiconductor device according to claim 23, wherein a major axis of the first shared contact and the end portion of the first gate electrode projecting from the first active area are arranged in the same direction, and

20 a major axis of the second shared contact and the end portion of the third gate electrode projecting from the third active area are arranged in the same direction.

25 25. A semiconductor device according to claim 19, wherein a gate width direction of the first MOS transistor and a gate width direction of the fourth MOS transistor are arranged at an angle of 20 to 30 degrees relative to the long side of the rectangular unit cell which is configured from the first to sixth MOS transistors.

26. A semiconductor device according to claim 19, wherein the first to fourth active areas are formed on an insulating film.